Quarterly report
Chronic Microelectrode Recording Array
NIH/NINDS
Period 09/30/04-12/31/04

Project: NIH/NINDS **Contract-No.** HHSN265200423621C
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I. Executive summary

The overall goal of the contract No. NIH/NINDS HHSN265200423621C is to develop and test (in-vivo) a chronically implantable neural recording array and provide the device to the neuroscience community upon completion of the initial technical development phase for experimental use and evaluation.

In order to accomplish this task, existing and new technologies are being merged. The chronic recording array will consist of a high density flip-chip integrated stack of modules: a thinned Utah Electrode Array (UEA), a CMOS based signal processor (low noise amplifier, peak detector) and communications module (forward and reverse telemetry link, RF module) and an LTCC[1] based high permeability ferrite coil for inductive power coupling. Silicon carbide and Parylene are intended for use as hermetic encapsulating material. The project is separated into an initial 18 month project phase during which the technical feasibility of the concept is to be shown in a four week in-vivo trial, followed by two twelve month and a final six month phase during which the device design and fabrication processes will be optimized, the long term stability increased and training and service procedures for device users will be incorporated.

The objective of the first quarter (Q1) as proposed was to:

a) establish the consortium and research team (sub-contracts, kick-off meetings, employ research associates and technicians where required, etc.)
b) evaluate potential failure modes and decide on the detailed design and processing strategies and materials used
c) procure equipment and set up test assemblies and fixtures
d) start design and development of the device modules and processes (signal processor, UEA, coil, flip-chip packaging and silicon carbide/Parylene encapsulation)
e) design and fabricate test structures for flip-chip process and coating material characterization

Throughout the first quarter, all the above mentioned objectives (a-e) were accomplished. Initial tests of materials and processes support the validity of the proposed device design and fabrication approach. In addition, a list of invention disclosures in preparation of US patent applications was made to the University of Utah Technology Transfer Office (TTO), protecting all key innovations (materials, design and processes) required for later commercialization of the device.

Furthermore, based on discussions with fellow researchers and NIH/NINDS officers at the Neuroprosthetics workshop in Bethesda, talks were commenced with potential additional collaborators in the field in order to maximize the information exchange between recording array users and technology providers. An official collaboration with Cyberkinetics Inc. to share know-how and propel later technology transfer is currently being discussed. A meeting with researchers at Case Western University, Cleveland, OH is planned for March 2005.

[1] LTCC- Low Temperature Co-fired Ceramics

II. Activity Summary

Key results for project period (Q I)

- Fabrication of ultra thin Utah Electrode Array: re-activation of fabrication processes, design of UEA handling tool for transportation and flip-chip bonding, tests for process modification of original UEA processes to 4 " wafer process
- Development and fabrication of electronics and communications module: establishing of CMOS signal processor design including forward and reverse telemetry module, power recovery module, A/D converter, multiplexer, spike detector and amplifier
- Development and fabrication of LTCC ferrite coil: electrical testing of initial LTCC coil properties provided by Fraunhofer IZM for a variety of geometries between 3.2 x 3.2 mm^2 and 6 x 6 mm^2
- Flip-chip bonding and assembly: selection of two (2) suitable flip-chip bond processes taking into account biocompatibility of materials and electrochemical similarity of metals to prevent corrosion effects, FMEA[2] of flip chip interconnect and bonding process, design and fabrication of flip-chip test structures emulating UEA and signal processor modules for metallization, bonding process and underfiller optimization
- Hermetic encapsulation and layer coating: procurement of Parylene CVD coater, selection of test program / accelerated ageing tests, FMEA of encapsulation and deposition process failure modes, design and fabrication of test structures for coating layer adhesion and electrical characterization (acute and long-term), deposition of silicon carbide and Parylene layers on test structures

Meetings/presentations during project period (Q I)

- Presentation of contract and project objectives at NIH/NINDS workshop on neuroprosthetics in Washington/Bethesda, Nov. 15-17, 2004
- Kick-off meetings: Univ. of Utah/Stanford University at NIH/NINDS workshop; Univ. of Utah/Fraunhofer IBMT (St. Ingbert, Germany, Nov. 18/19, 2004); Univ. of Utah/Fraunhofer IZM (Berlin, Germany, Nov. 22/23, 2004)
- Individual weekly project meetings of the project teams at the University of Utah as well as the subcontractors; meeting minutes are created in common format by all partners.

Patents (Q I)

- Invention disclosure to University of Utah Technology Transfer Office (TTO) for the following patents:
    - A chronically implantable integrated neural interface
    - Hermetic encapsulation of neuroprosthetic implants using silicon carbide
    - High density Flip-chip packaging integration for neuroprosthetic devices
    - Use of LTCC-based ferrite material and coils for implantable devices
    - Hexagonal geometry for UEA for high density packing of electrodes

Organizational accomplishments (Q I)

- Employment of graduate students and technician for project
- Establishment of subcontracts (not signed, yet), reporting, meetings minutes and FMEA forms

[2] FMEA-Failure Mode Effects Analysis: a quality management analysis tool

III. Research Results and Discussion

III.a. Probe system fabrication

III.a.1 Task 1 Fabrication of ultra thin Utah Electrode Array

Description/Rationale

As a first step towards the fabrication of ultra thin Utah Electrode Arrays, the existing processes were documented, reviewed and partially re-activated. No further activities were planned for the first quarter.

Future plans for the next two (2) quarters

In the coming two quarters, the polishing process will be established for electrode arrays with baseplate thickness of a) about 100 µm and b) about 20-30 µm. Characterization of mechanical stability and impact on electrical properties due to thinning of baseplate during flip-chip bonding and device operation.

III.a.2 Task 2: Development and fabrication of electronics and communications module

Description/Rationale

The electronics/communication module will take the form of a single CMOS integrated circuit mounted on the back of the microelectrode array. Additionally, we are planning to use three surface-mount passive devices – capacitors and an inductor – mounted near the chip to provide capacitance and inductance values not achievable on chip. The electronics/communication module will amplify and process neural signals, transmit this data out of the body on an RF carrier, and receive power and command data from the LTCC coil via a transcutaneous magnetic link.

Experimental Results

We have completed an initial architecture design for the version 1 integrated circuit. The chip will measure approximately 5 mm × 5 mm × 220 µm, and will consist of the following functional components:

- **Power recovery module.** This module will interface with the LTCC coil and convert the unregulated ac voltage on the coil into a regulated dc voltage to power the chip. We will use an on-chip full-wave bridge rectifier to convert ac to dc. A linear voltage regulator with a bandgap voltage reference will be used to regulate the power supply voltage at 3.3 VDC. We will use an ac power signal in the 1 MHz – 5 MHz range.
- **Forward telemetry module.** This module will also interface with the LTCC coil and perform two functions. First, this circuit will generate a stable, digital (square wave) clock synchronized to the oscillation on the coil. This clock will serve as a frequency reference for the entire chip. Second, this circuit will identify changes in the amplitude of the ac voltage waveform on the coil. These amplitude changes will be used to send telemetry data (e.g., configuration commands) to the implanted device. This circuit will interpret each amplitude change as a 'one' or 'zero', and load this binary data stream into on-chip configuration and command registers.
- **Neural signal amplifiers and spike detectors.** A 10 × 10 array of neural signal amplifiers and spike detector circuits will form a 4 mm × 4 mm array at the center of the chip. Each amplifier will have an octagonal bond pad 70 µm in diameter that will connect to the microelectrode array. Each amplifier will have a gain of 60 dB and a bandwidth from 300 Hz (to block large-amplitude local field potentials) to 5 kHz. A comparator will be used to detect spikes by comparing the output of the neural amplifier to a programmable reference level set by an on-chip digital-to-analog converter (DAC).

- **Analog MUX and ADC.** The chip will have a 10-bit analog-to-digital converter (ADC) to digitize a selected neural waveform at 15 kSamples/s. An analog multiplexer (MUX) will be used to route the selected neural amplifier signal to the ADC. Initial versions of the charge-redistribution ADC have already been fabricated and tested.
- **RF transmitter for reverse telemetry.** We will build an on-chip RF transmitter to transmit the digital data from the ADC and the spike detectors. The transmitter will operate near the 433 MHz ISM band and will transmit data at a rate of 330 kbit/s using either binary amplitude-shift keying (ASK) or frequency-shift keying (FSK). We will use an off-chip surface-mount high-Q inductor to minimize power consumption by the transmitter. We have recently acquired a Texas Instruments TRF6903 single-chip multiband RF transceiver chip that may be used to build the non-implanted telemetry receiver.

Discussion/Interpretation of Results

The proposed chip architecture should allow for a fully-functional integrated neural interface. However, we will make the initial design modular so that each component can be tested separately. This will allow us to work around any subcircuits that do not work as expected in the benchtop tests, and determine the cause of failure so that it can be corrected in version 2 of the chip.

Initial tests of the integrated charge-redistribution ADC show an integral nonlinearity error (INL) of ±6 LSB over a range of 0.7 V – 3.2 V when powered from a 3.3 V supply. We have submitted a revised version of the ADC for fabrication which should have lower INL error. Simulations indicate that the ADC module will consume less than 7 μW of power.

Future Plans for Next Two (2) Quarters

Design, simulation, and layout for version 1 of the integrated circuit is currently underway. The chip will be submitted to the MOSIS service for fabrication on March 14, 2005. The chip will be fabricated in AMI Semiconductor's 0.5-μm 2-poly, 3-metal CMOS process. We expect to receive the fabricated chips around mid to late May. We will receive 40 copies of the chip; ten of these will be packaged in ceramic chip carriers to facilitate benchtop testing. The remaining 30 bare die will be used to test the assembly and coating steps.

Benchtop testing will commence upon receipt of the packaged chips. After testing the chip in June and July, we will begin design of version 2 of the chip, which will address any shortcomings found in version 1. This chip will be submitted for fabrication in August or early September, and should return from fabrication in October or November 2005.

III.a.3 Task 3: Development and fabrication of LTCC ferrite coil

Description/Rationale

An LTCC (low-temperature coefficient ceramic) coil will be used to receive the magnetic ac power waveform transmitted through the skin. The coil will measure approximately 5 mm × 5 mm, and will be mounted above the integrated circuit.

Experimental Results

In December, we received five types of test coils from Robert Hahn at the Fraunhofer Institute IZM. These coils are shown in the figure below:

Figure 1: LTCC coils, types R-V (U.S. dime shown for scale)

We have measured the basic electrical properties of these coils using an SR715 LCR meter. The results are presented in table form below:

Table I: LTCC Coil Measurements

Coil type	Dimensions (mm)	Number of turns	Measured inductance (nH)	Series resistance (Ω)	Q at 1 MHz
R	3.5 × 3.5	5	180	0.74	1.5
S	4.0 × 4.0	5	160	0.41	2.5
T	3.2 × 3.2	3	60	0.14	2.7
U	4.8 × 4.4	4	140	0.25	3.5
V	6.0 × 6.0	5	240	0.38	4.0

Discussion/Interpretation of Results

The series resistance of the coils is low enough to yield reasonably high Q values at the expected operating frequency of 1 MHz. In order to test the coils in a realistic setting, we need to attach wires so that circuits may be built simulating the power recovery module in the integrated circuit, and we can provide a 1-MHz magnetic field using a class-E transmitter. Initial attempts at soldering wires to the coils have failed, and we are currently in the process of acquiring silver-epoxy adhesive to accomplish this task.

Future Plans for Next Two (2) Quarters

After we have attached wire to the test coils, we will begin experiments using a class E power transmitter (currently under design) and transmitting coil. These experiments will determine the voltage amplitude it is possible to achieve across the LTCC coil with inter-coil spacings similar to those in implanted situations.

III.a.4 Task 4: Flip-chip bonding and assembly

Description/Rationale

Two different flip chip bonding techniques are chosen for the mounting of the IC on the UEA: AuSn reflow soldering (version A) and as an alternative solution thermocompression bonding (version B). The requirements for the packaging in the initial project phase are above all the reliability aspects, the miniaturization, the use of biocompatible materials and the choice of an applicable process flow combining the demands for IC, SMD as well as LTCC mounting.

Experimental Results

As a basis for the accomplishment of the packaging an adequate handling tool for the fixing and protection of the spices will be provided by the University of Utah (see next section below). The metallization of the UEA bond pads were selected and first silicon test samples were manufactured to investigate on the one hand the bondability of the metallization and the underfilling process. The evaluated process flow applying AuSn reflow soldering is presented in the table below:

Table II: Process flow for version A

	Process step	**Description**
1.	AuSn bumping	ICs will be provided as single chips; electroplating will be used for bumping
2.	IC assembling	Reflow soldering of the IC on the UEA
3.	underfilling	Underfilling of the gap between IC and UEA
4.	SMD mounting	Dispensing of solder or adhesive for SMD mounting
5.	LTCC mounting	Dispensing of solder or adhesive for LTCC mounting
6.	underfilling	Underfilling of the gap between LTCC and IC

The difference in process flow between the AuSn bonding and the alternative thermocompression bonding is the IC bumping and assembling. The bumping can be done either by electroplating or by Au stud bumping. Force and temperature will be used during bonding to achieve a welding between Au bump and UEA pad. Figure 2 illustrates the package concept.

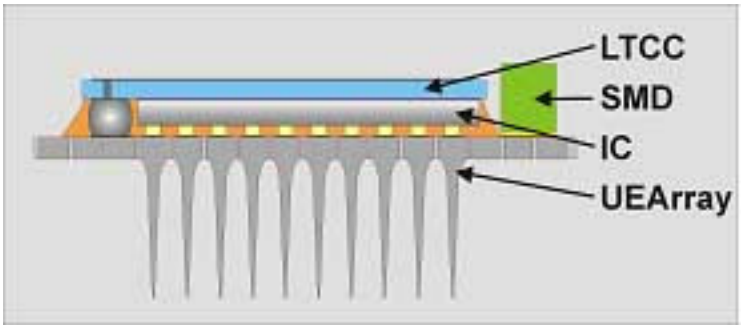


Figure 2: schematic of the package concept, the underfiller is shown in orange

Discussion/Interpretation of Results

The preferred bumping method for the IC would be AuSn reflow soldering. The advantage compared to thermocompression bonding is the lower force during assembling which minimizes stress on the UEA.

Future Plans for Next Two (2) Quarters

The IC test samples will be used to investigate the chosen bond pad metallization. Underfiller materials for gaps between 25 and 30 µm will be selected and tests will be performed. First assembling tests using the UEA handling tool will give information about the maximum applicable stress and the heat transfer through the tool and the UEA during bonding. Both parameters (force and temperature) will mainly influence the package bonding processes.

Subtask: handling tool

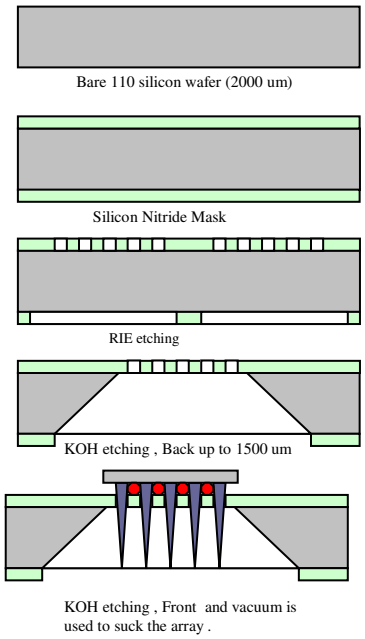
Description /Rationale

Flip-chip bonding and transportation of the electrode arrays requires a special handling tool that protects the delicate electrode tips of the array. The key challenges are the temperature and pressure exerted on the array during flip chip bonding. Depending on the process employed, the forces applied on a die can be of the order of a few 10 N at temperatures of up to 400 °C. Prior to designing the handling tool, the baseplate thickness uniformity of conventional Utah Electrode Arrays was analyzed in order to identify potential failure modes and priorities for fabrication process improvement (Figure 3). Since the glass insulation

material protrudes in between the Silicon spikes, a handling tool can be designed that will be in contact with the glass sections only and not touch or damage the silicon spikes.

Figure 3: cross sectional view of conventional Utah Electrode Array for analysis of base plate thickness uniformity. Encapsulation process and polishing lead to slight bending of the electrode spikes. Due to the smaller etch rate of the glass compared to silicon, the glass protrudes in between the Silicon spikes.

Prior to deciding on a handling device design, a variety of different approaches were evaluated and discarded. The schematic design and process flow for the current version of the handling tool is shown below (Figure 4).



The keynote in this design is to ensure that the array rests on the glass partition between the arrays rather than on the needles. This will ensure that no undue stress is induced on the needles which might cause them to crack.
The specific device design requires use of anisotropic bulk micromachining using KOH. A special setup was built for very high homogeneity and accuracy etching. The process was fully characterized and qualified. The following parameters are used for the bulk micromachining:

1. Etchant: Premix Potassium Hydroxide (KOH, 40 %) for 100 Silicon
2. Etch rate: 1 mil/3 min.
3. Bath Temperature 100 Degree C.

A schematic of the KOH setup used is graphically shown in Figure 5.

Figure 4: Schematic design and process flow for electrode array handling tool

Future plans for next two (2) quarters

During the next two quarters we are planning to finish fabrication and testing of the handling devices and fabricate a supply of re-usable handling tools for the entire project length.

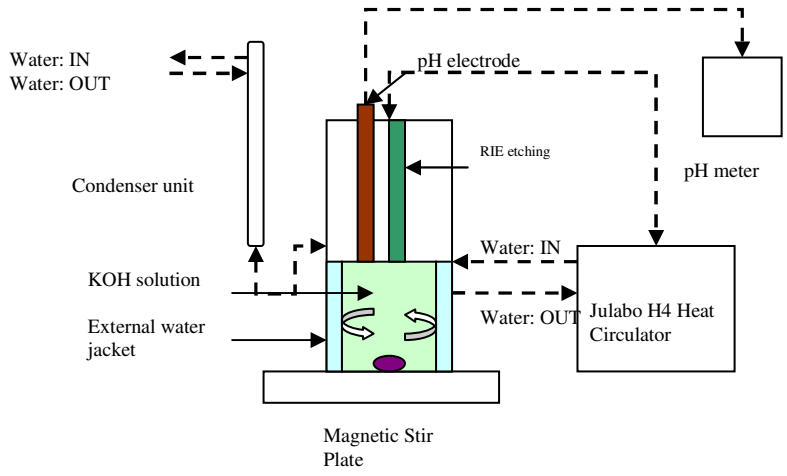


Figure 5: Schematic KOH bulk micromachining setup

Subtask: flip-chip test structures

Main Tasks Accomplished

The purpose of this subtask is to fabricate the under-bond metallization (UBM) layers for use in flip-chip bonding trials.

1. mask development for UBM patterning
2. fabrication of initial Al and Ti/Pt/Au flip-chip test structures

Description/Rationale

The flip-chip bonding process will be critical to fabrication of a compact, highly integrated, and biocompatible neural array. Issues regarding mechanical strength, corrosion resistance, and biocompatibility of the flip-chip interconnections need to be investigated to optimize this process and generate a device with reasonable *in vivo* lifetimes. Test structures consist of 10×10 arrays of equilateral octagons that are 70 µm across (flat-to-flat), and are spaced with a 400 µm pitch like the probes of the array. This yields an overall die that is 5 mm on a side. In addition, 200×200 µm cross features are include to indicate the scribe alleys used to dice the wafers. Fig. 6a-b are pictures of the (a) the overall mask layout for one complete die, and (b) a close-up illustrating the octagon shape of the bond pads.

(a) (b)

Fig. 6 a-b. Mask file for patterning the UBM metallization. (a) Image of a complete die and (b) close-up of the individual octagons in the array.

This mask is used to pattern layers of Al and Ti/Pt/Au to generate the bond pads. The Al layers are nominally 1.7 µm thick to match those produced by the foundry producing the CMOS signal processing chips. The Ti/Pt/Au metallization scheme with thicknesses of 500/2400/2000 Å is similar to the existing semiconductor contact scheme used on previous generations of the neural array with the addition of a Au layer used for compatibility with the solder bump process. The Al structures are patterned with standard Al etching techniques. The Ti/Pt/Au metallization is patterned by lift-off due to the difficulty in etching the noble metals Pt and Au. The patterned UBM layers will be used for trials to evaluate the flip-chip process by IZM in Germany.

Experimental Results

Both bright-field and dark-field masks were generated for etching Al and lift-off of Ti/Pt/Au metallizations, respectively. Each mask is 5" × 5" for patterning 4" silicon wafers, and has a 20 × 20 array of individual die across the mask. Subsequent measurement of the octagons by optical microscopy indicates they have the correct dimensions as specified by the mask illustrated in Fig. 6.

The Al films were deposited in a recently acquired sputter deposition manufactured by TM-Vacuum. The load-lock and deposition chambers are pumped by separate CTI cryopumps for high-vacuum, and by a common dry pump for rough vacuum, and reached a base pressure of 4×10^{-7} Torr prior to deposition. For deposition, UHP Ar was introduced to the system at 150 sccm, which in combination with a throttle valve controlled pressure at 5 mTorr during deposition. A 3" planar magnetron sputtering source with a 99.99% Al target was used to deposit the films with 150 W of power onto the rotating 4" wafer. A series of thickness measurements taken across the substrate by stylus profilometry indicate the film thickness is non-uniform across the substrate, and therefore requires further optimization. The metallized wafer is patterned by standard photolithography with a commercial Al etchant. Measurements by optical microscopy indicate the patterned features are smaller than those on the photomask; therefore, the photolithography process requires further optimization.

For the Ti/Pt/Au layer fabrication where the lift-off process is used, the first step is to spin photoresist (Shipley 1813) onto the wafer, followed by exposure and development. This yields windows in the resist where the metal will adhere to the substrate. The multilayer films were deposited in a Denton Discovery 18 sputter deposition. The base pressure was 7×10^{-7} Torr achieved by a turbo-molecular pump backed by a rotary vane pump. For deposition, UHP Ar was introduced at 15 sccm and 30 sccm for the Ti and Pt/Au layers, respectively. Each layer was deposited at 50 W to minimize heating of the photoresist-coated substrate. The three high purity targets were placed in separate 3" planar magnetron sources, and the wafer was rotated to achieve uniform film thickness across the substrate. After deposition, the substrate is soaked in Acetone to remove the remaining photoresist, and the metal on top. A picture of some resulting octagons is presented in Fig. 7.

Stress and adhesion problems can result in some die having misshaped features, therefore further optimization is needed for a reliable lift-off process to increase yields of successful die. Initial samples of wafers with both Al and Ti/Pt/Au pads were sent to IBMT in Germany for initial flip-chip experiments.

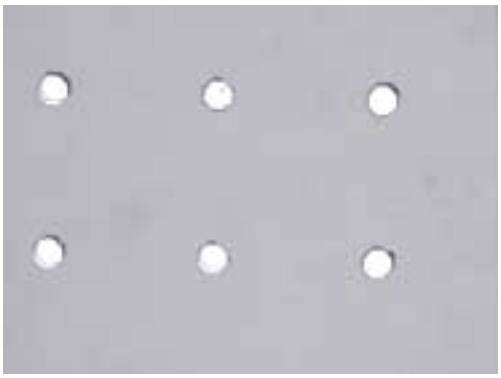


Fig. 7: Optical micrograph of Ti/Pt/Au octagons patterned on an oxidized silicon wafer substrate.

Future plans for the next two (2) quarters

Over the coming quarters, we will work to improve our photolithography to improve the yields of successful die with metal pads that have the correct dimensions across the entire wafer. Additional work will also focus on controlling stress in the deposited layer to improve adhesion of the layers. In addition, the deposition geometry will be modified in the TM-Vacuum system to optimize the uniformity in film thickness across the 4" diameter substrates. Several surface modification techniques will be investigated to improve adhesion of the metallization layers to improve the lifetime of the subsequent solder bumps, and decrease their susceptibility to mechanical damage. We will also perform more characterization on the bond pads to investigate their electrical and structural properties, and composition. These data can be compared to results taken after solder bumping to investigate changes in the UBM layer, and provide feedback to optimize the UBM and solder bumping processes.

III.a.5 Task 5: Hermetic encapsulation and layer coating

Main subtasks accomplished:

1. Failure Mode Effects Analysis (FMEA) to determine most likely failure modes and action priorities for the encapsulation layers and deposition processes prior to starting processing (FMEA document is available to NIH/NINDS upon request at any time)
2. Design and fabrication of test structures to characterize adhesion and hermeticity of the layers towards alkaline ions and humidity as function of surface treatment, deposition layers and process parameters
3. Deposition of SiC and Parylene layers on test structures
4. Procurement of Parylene coater (delivery scheduled for first quarter 2005)

Description/Rationale

According to the FMEA the most likely failure modes for a coating material are chemical biocompatibility, which can be mitigated using the SEMI-spec cleaned surfaces and the right materials, adhesion problems, which is primarily influenced by processing parameters and ion or humidity penetration through the coating leading to corrosion effects underneath the passivation.

In order to characterize and compare the impact of the surface cleaning and material deposition process parameters prior to applying the encapsulation layers on the complete device, silicon based interdigital electrode test structures were designed and fabricated. The design concept of the test chip is to mimic the UEA structure. Thus the interdigital electrode pitch as well as coating material is a duplication of UEA geometry (i.e. a pitch of 400 µm) and materials (i.e. Ti/Pt metallization and SiC, Parylene C and Parylene C on SiC coatings). Accelerated ageing tests (pressure cooker and heater saline solution) are performed to determine and analyze potential failure modes for the layers. Using impedance spectroscopy the following failure mode on coating material as well as electrode metallization could be envisioned by this acceleration test:

1. Adhesion failure or ion or humidity penetration into the interface between layer and device leading to corrosion of metallization and short circuits
2. Degradation or property change of protection layer bulk

Experimental Results

We have established stable fabrication parameters and fabricated test chips. The test chip feature metal interdigital comb structures on SiO_2 wet thermal oxide for insulation. Patterning is done using lift-off. The metallization layer sequence consists of Ti (50 nm) and Pt (240 nm) mimicking the UEA bondpad metallization scheme or alternatively Ti(50 nm)/Pt(240 nm)/Ti(100 nm)/Ir(200 nm) resembling the

electrode tip metallization. First tests were conducted depositing the following encapsulation layers on the test structures:

1. PECVD SiC layers (1-3 µm)
2. CVD Parylene C layers (2-5 µm)

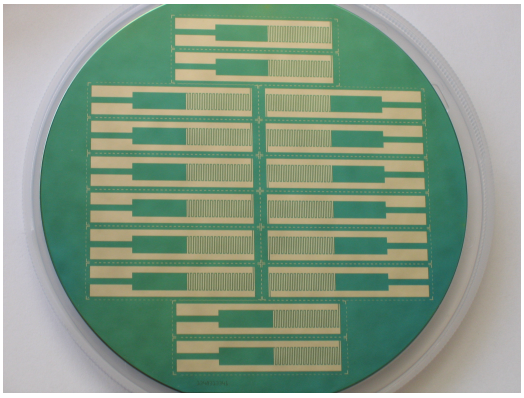


Figure 8: 4" wafer with fabricated layer test structures (Ti 50 nm / Pt 240 nm)

Future plans for next two (2) quarters

In the coming two quarters we are planning to:

1. vary the surface treatment processes (RIE/plasma etching) prior to deposition for improved interface cleanliness between device and encapsulation layers
2. deposit double layers of PECVD SiC and CVD Parylene C layers
3. perform adhesion, leakage current and impedence spectroscopy tests on single and double layers as acute and accelerated aging tests in heated saline solution / pressure cooker in collaboration with Fraunhofer IBMT
4. optimize the deposition parameters and select optimum coating material and deposition parameters

III.a.5.1 SiC coating

Description/Rationale

The Silicon Carbide coating is being carried out on a Plasma Enhanced Chemical Vapor Deposition system (PECVD). The key objective is to obtain highly dense, low stress SiC layers at low deposition temperatures (< 250 °C) in order to prevent damage to polymeric flip-chip underfiller materials during deposition. First layers were deposited on test structures. Layer composition analysis is required to obtain high layer density, low defect density, high dielectric constant and low etch rate in saline solution.

Experimental results

The layer composition was analyzed using EDX[3]. The flow rates used were as follows:

1. Methane: 14.6 sccm
2. Silane: 4.8 sccm
3. Hydrogen:51.1 sccm which is then increased to 60.5 sccm after 8 minutes.

The substrate temperature used was 315° C at an RF power of 4.5 Watts and a pressure of 350 mtorr. Examples of initial results are given in Table III:

[3] EDX – electron dispersive x-ray spectroscopy

Table III: EDX-Analysis of PECVD SiC layer composition

Sample Number	Element	Wt%	At %
GD1	C	19.47	26.69
	O	58.66	60.37
	Si	17.25	10.11
GD2	C	18.48	25.18
	O	61.83	63.24
	Si	15.15	8.83
GD3	C	12.87	25.35
	O	1.95	2.88
	Si	84.44	71.12

Discussion/Interpretation of results

The EDX data of the preliminary runs shows a high amount of Carbon which inferred that we were flowing excess of Methane in the reaction. With a subtle adjustment in the flow rates of Methane, Silane and Hydrogen we were able to bring up the Silicon content by the third run. Thus, further adjustment in the flow rates is required to obtain the desired amount of Silicon and Carbon in the film, which is our next step for the deposition. The results will then be analyzed using EPMA and EDX to corroborate the results.

Future plans for next two (2) quarters

During the coming two quarters we will fine tune the layer composition (Si and C content), characterize the chemical and dielectric properties as well as the step coverage and adhesion of the layers. The layers will be deposited on the interdigital comb test structures to perform accelerated aging tests of the layers in saline solution.

III.a.5.2 Parylene coating

Description/ Rationale

The Parylene electrical and mechanical/adhesion properties on SiC, SiO_2 and thin film metals such as Pt need to be characterized and optimized. Thus, platinum test structures on silicon substrate were fabricated for a first investigation of the Parylene C layer adhesion to the substrate and for long term reliability testing. The geometry of the test structures is shown in figure 8. After this first evaluation, additional test structures coated with silicon carbide will be fabricated, coated with Parylene C and tested in order to check a) adhesion and electrical properties of the Parylene C on an inner SiC layer and b) characterize the chemical and electrical stability of double layer stacks consisting of an innermost SiC and an additional Parylene layer. This way the most likely layer combinations to be successful as long term encapsulation will be evaluated: SiC, Parylene C and Parylene C on SiC. Parylene C is chosen as the encapsulation material because of its superior biocompatibility and low moisture uptake in comparison with other parylene variants such as parylene N and parylene D. A *Paratech Lab Top 3000* coating system is used for parylene C deposition at Fraunhofer IBMT. An identical system is being installed at the University of Utah. Fig. 9 and 10 show the vials and setup used for in-vitro analysis of the materials on test structures.

Experimental Results

No significant experimental results can be reported, yet, other than successful CVD coating of the first test structures.

Discussion / Interpretation of results

n/a

Fig. 9: sample bottle and connector cap (bottle opening diameter is 1 cm).

Fig. 10: coating material test setup with temperature controlled mounting block for samples; the block temperature is maintained at 37°C by hot water circulation; screen shows analysis software (leakage current vs time (red line).

Future plans for the next (2) quarters

Typically, Parylene C adhesion to noble metals such as platinum, gold etc. is poor. To improve adhesion of the Parylene C layer to the platinum and silicon carbide test structures, a combination of various surface modification/cleaning methods such as adhesion promoters and plasma assisted surface modification/cleaning will be investigated. The adhesion properties will be quantified using shear- and tensile strength tests.

We have also planned the evaluation of leakage currents between electrodes and through the bulk passivation on a long term basis for assessment of the reliability of the various Parylene C coatings. The aforementioned test structures are used for this purpose. The test uses a bias voltage of + 5 VDC across the samples and leakage currents through the samples maintained at 37°C in 0,9% NaCl solution are measured at regular time intervals. The result will be used for understanding different modes of failure of the encapsulation layer and optimization of the layers.

III.a.5.3 double layer coating

n/a in first quarter, planned for third quarter

III.b.1 Task 6: Testing and validation of probe systems (in-vitro/in-vivo)

n/a at this stage of the project except for definition of test program

III.b.1.1 Bench testing of interface/electronics

n/a at this stage of the project

III.b.1.2 In-vivo testing of interface

No in-vivo testing at this stage of project

III.b Concerns

No major deviations or delays have occurred during the first quarter. We would however like to notify NIH/NINDS of two slight deviations from the original plan which from current perspective do not impact the schedule and outcome of the project:

1. The subcontracts with Stanford as well as the German subcontractors Fraunhofer IZM and IBMT have been fully negotiated and completed, but not signed, yet. Signatures are expected during the first weeks of January. This issue has not had any impact on the actual work packages being performed, since all sub-contractors have commenced work on their respective work packages as scheduled in the proposal even without signed contract. The kick-off meetings have been scheduled and held at the first possible date in November upon awarding of the contract.

2. The technican YanPing Li Zhang, who was responsible for the fabrication of the original Utah Electrode Array and who was supposed to take over fabrication of the thinned Utah Electrode Arrays has at short notice resigned from her position by the end of November 2004 to accept a new job offer. In order to mitigate the risk of delays the following immediate actions were taken:

a. posting of a job opening for a suitable technician and conducting of interviews with 5 eligible candidates (December 2004), filling of the position is expected in January 2005
b. creation of clear documentation and "cook-book" for the array fabrication
c. training of a graduate student to ensure continuity of the fabrication know how and create redundancy in the team for array fabrication. This student will also be involved in the optimization of the electrode array fabrication process and the development of the new thinning process, thus leading to significant team synergy effects
d. reaching of an agreement with the former employee YanPing Li Zhang to continue supporting the project for up to 6 months during evenings and weekends

Salt Lake City, Utah, January 7th 2005

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